

# CS8182

## Micropower 200 mA Low Dropout Tracking Regulator/Line Driver

The CS8182 is a monolithic integrated low dropout tracking regulator designed to provide an adjustable buffered output voltage that closely tracks ( $\pm 10$  mV) the reference input. The output delivers up to 200 mA while being able to be configured higher, lower or equal to the reference voltages.

The device has been designed to operate over a wide range (2.8 V to 45 V) while still maintaining excellent DC characteristics. The CS8182 is protected from reverse battery, short circuit and thermal runaway conditions. The device also can withstand 45 V load dump transients and  $-50$  V reverse polarity input voltage transients. This makes it suitable for use in automotive environments.

The  $V_{REF}/ENABLE$  lead serves two purposes. It is used to provide the input voltage as a reference for the output and it also can be pulled low to place the device in sleep mode where it nominally draws less than  $30 \mu\text{A}$  from the supply.

### Features

- 200 mA Source Capability
- Output Tracks within  $\pm 10$  mV Worst Case
- Low Dropout (0.35 V Typ. @ 200 mA)
- Low Quiescent Current
- Thermal Shutdown
- Short Circuit Protection
- Wide Operating Range
- Internally Fused Leads in SO-8 Package
- For Automotive and Other Applications Requiring Site and Change Control
- Pb-Free Packages are Available

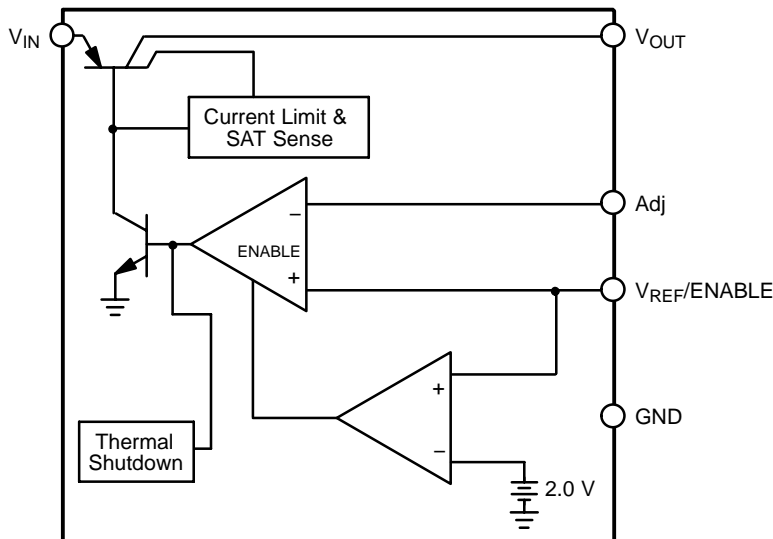
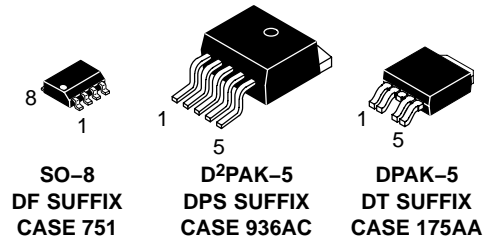


Figure 1. Block Diagram

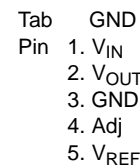
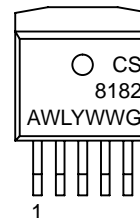
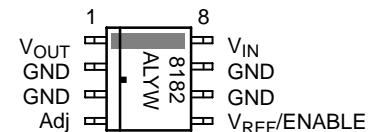


ON Semiconductor®

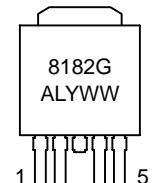
<http://onsemi.com>



### PIN CONNECTIONS AND MARKING DIAGRAMS



Tab GND  
Pin 1.  $V_{IN}$   
2.  $V_{OUT}$   
3. GND  
4. Adj  
5.  $V_{REF}$



A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G or ■ = Pb-Free Device

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

# CS8182

## PACKAGE PIN DESCRIPTION

Package Lead Number			Lead Symbol	Function
SO-8	D <sup>2</sup> PAK 5-PIN	DPAK 5-PIN		
8	1	1	V <sub>IN</sub>	Input Voltage
1	2	2	V <sub>OUT</sub>	Regulated Output
2, 3, 6, 7	3	3	GND	Ground
4	4	4	Adj	Adjust Lead
5	5	5	V <sub>REF/ENABLE</sub>	Reference Voltage and ENABLE Input

## MAXIMUM RATINGS

Rating	Value	Unit
Storage Temperature Range	-65 to +150	°C
Junction Temperature	+150	°C
Supply Voltage Range (Continuous)	-16 to 45	V
Peak Transient Voltage (V <sub>IN</sub> = 14 V, Load Dump Transient = 31 V)	45	V
Voltage Range (Adj, V <sub>OUT</sub> , V <sub>REF/ENABLE</sub> )	-10 to +V <sub>IN</sub>	V
Package Thermal Resistance, SO-8: Junction-to-Case, R <sub>θJC</sub> Junction-to-Air, R <sub>θJA</sub>	25 80	°C/W °C/W
Package Thermal Resistance, D <sup>2</sup> PAK Junction-to-Case, R <sub>θJC</sub> Junction-to-Air, R <sub>θJA</sub>	4.0 48	°C/W °C/W
Package Thermal Resistance, DPAK Junction-to-Case, R <sub>θJC</sub> Junction-to-Air, R <sub>θJA</sub>	8.0 64	°C/W °C/W
ESD Capability (Human Body Model) (Machine Model)	2.0 200	kV V
Lead Temperature Soldering: (Note 1)	(SO-8) (D <sup>2</sup> PAK) (DPAK) 240 225 260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 60 second maximum above 183°C.

## RECOMMENDED OPERATING RANGES

Rating	Value	Unit
Junction Temperature, T <sub>J</sub>	-40 to +125	°C
Input Voltage, Continuous V <sub>IN</sub>	3.4 to 45	V

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**ELECTRICAL CHARACTERISTICS** ( $V_{IN} = 14\text{ V}$ ;  $V_{REF}/ENABLE > 2.75\text{ V}$ ;  $-40^{\circ}\text{C} < T_J < +125^{\circ}\text{C}$ ;  $C_{OUT} \geq 10\ \mu\text{F}$ ;  
 $0.1\ \Omega < C_{OUT-ESR} < 1.0\ \Omega$  @ 10 kHz, unless otherwise specified.)

Parameter	Test Conditions	Min	Typ	Max	Unit
<b>Regular Output</b>					
$V_{REF} - V_{OUT}$ V <sub>OUT</sub> Tracking Error	$4.5\text{ V} \leq V_{IN} \leq 26\text{ V}$ , $100\ \mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$ , Note 2	-10	-	10	mV
	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 30\text{ mA}$ , $V_{REF} = 5.0\text{ V}$ , Note 2	-5.0	-	5	mV
Dropout Voltage ( $V_{IN} - V_{OUT}$ )	$I_{OUT} = 100\ \mu\text{A}$	-	100	150	mV
	$I_{OUT} = 30\text{ mA}$	-	-	500	mV
	$I_{OUT} = 200\text{ mA}$	-	350	600	mV
Line Regulation	$4.5\text{ V} \leq V_{IN} \leq 26\text{ V}$ , Note 2	-	-	10	mV
Load Regulation	$100\ \mu\text{A} \leq I_{OUT} \leq 200\text{ mA}$ , Note 2	-	-	10	mV
Adj Lead Current	Loop in Regulation	-	0.2	1.0	$\mu\text{A}$
Current Limit	$V_{IN} = 14\text{ V}$ , $V_{REF} = 5.0\text{ V}$ , $V_{OUT} = 90\%$ of $V_{REF}$ , Note 2	225	-	700	mA
Quiescent Current ( $I_{IN} - I_{OUT}$ )	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 200\text{ mA}$	-	15	25	mA
	$V_{IN} = 12\text{ V}$ , $I_{OUT} = 100\ \mu\text{A}$	-	75	150	$\mu\text{A}$
	$V_{IN} = 12\text{ V}$ , $V_{REF}/ENABLE = 0\text{ V}$	-	30	55	$\mu\text{A}$
Reverse Current	$V_{OUT} = 5.0\text{ V}$ , $V_{IN} = 0\text{ V}$	-	0.2	1.5	mA
Ripple Rejection	$f = 120\text{ Hz}$ , $I_{OUT} = 200\text{ mA}$ , $4.5\text{ V} \leq V_{IN} \leq 26\text{ V}$	60	-	-	dB
Thermal Shutdown	GBD	150	180	210	$^{\circ}\text{C}$
<b><math>V_{REF}/ENABLE</math></b>					
Enable Voltage	-	0.80	2.00	2.75	V
Input Bias Current	$V_{REF}/ENABLE$	-	0.2	1.0	$\mu\text{A}$

2.  $V_{OUT}$  connected to Adj lead.

TYPICAL CHARACTERISTICS

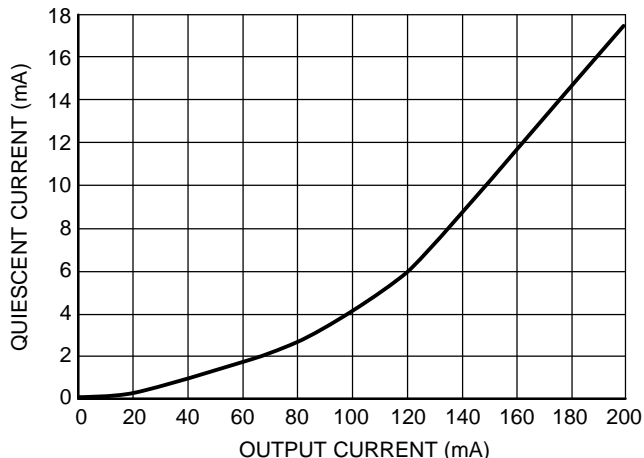


Figure 2. Quiescent Current vs. Output Current

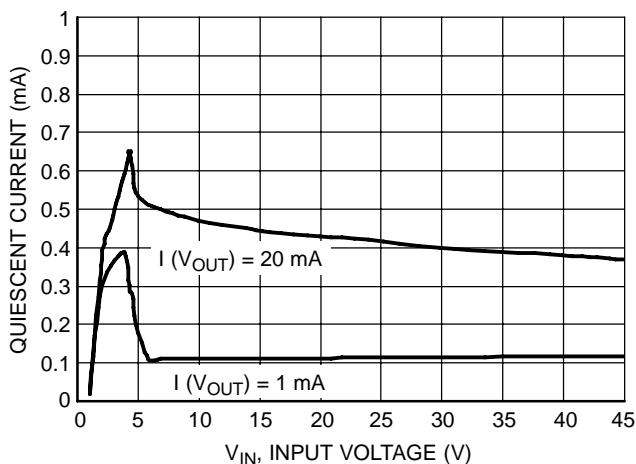


Figure 3. Quiescent Current vs. Input Voltage (Operating Mode)

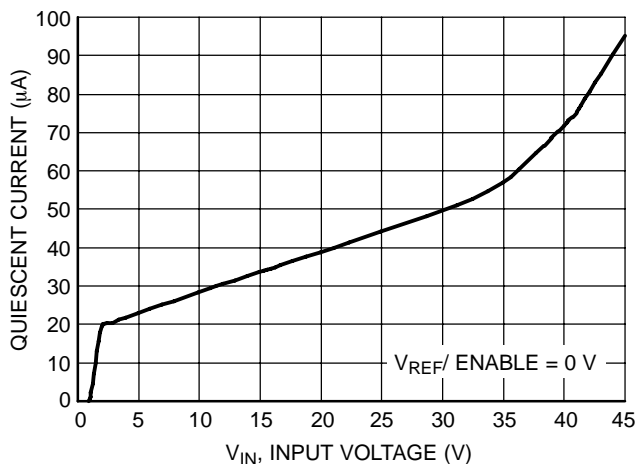


Figure 4. Quiescent Current vs. Input Voltage (Sleep Mode)

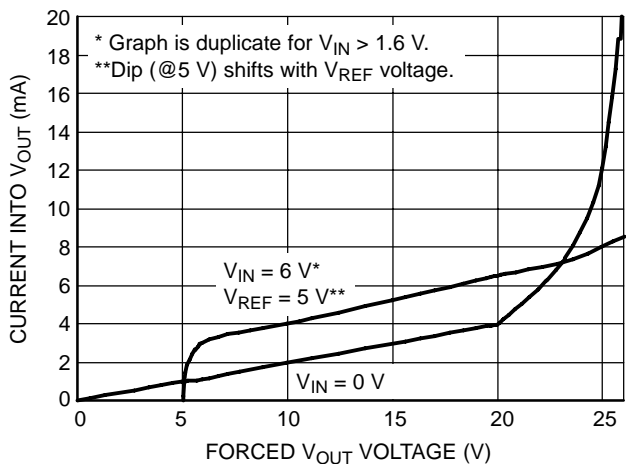


Figure 5.  $V_{OUT}$  Reverse Current

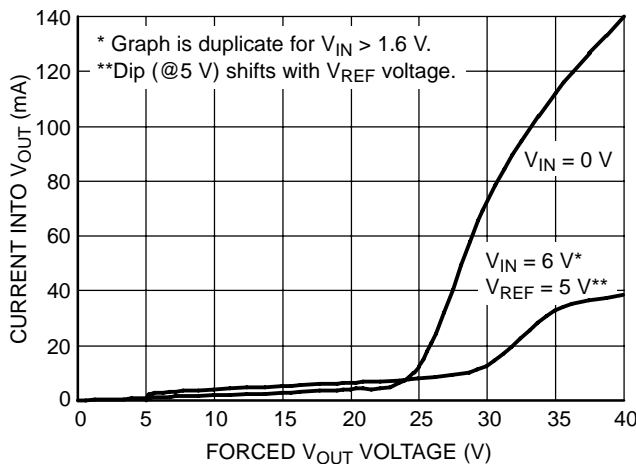


Figure 6.  $V_{OUT}$  Reverse Current

CIRCUIT DESCRIPTION

ENABLE Function

By pulling the V<sub>REF</sub>/ENABLE lead below 2.0 V typically, (see Figure 10 or Figure 11), the IC is disabled and enters a sleep state where the device draws less than 55 μA from supply. When the V<sub>REF</sub>/ENABLE lead is greater than 2.75 V, V<sub>OUT</sub> tracks the V<sub>REF</sub>/ENABLE lead normally.

Output Voltage

The output is capable of supplying 200 mA to the load while configured as a similar (Figure 7), lower (Figure 9), or higher (Figure 8) voltage as the reference lead. The Adj lead acts as the inverting terminal of the op amp and the V<sub>REF</sub> lead as the non-inverting.

The device can also be configured as a high-side driver as displayed in Figure 12.

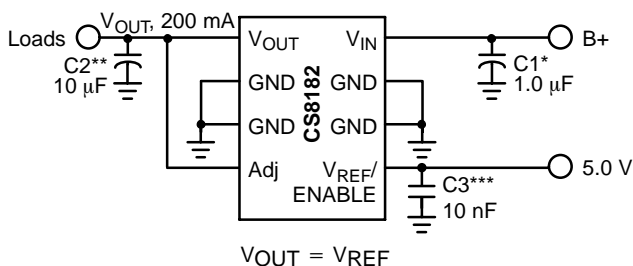


Figure 7. Tracking Regulator at the Same Voltage

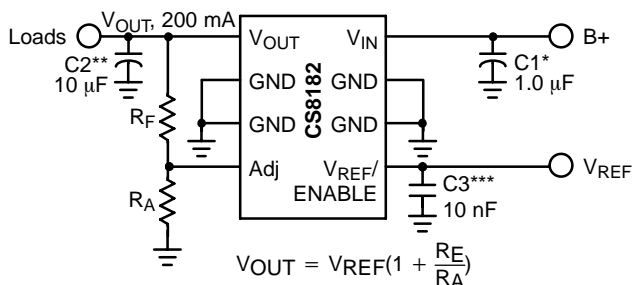


Figure 8. Tracking Regulator at Higher Voltages

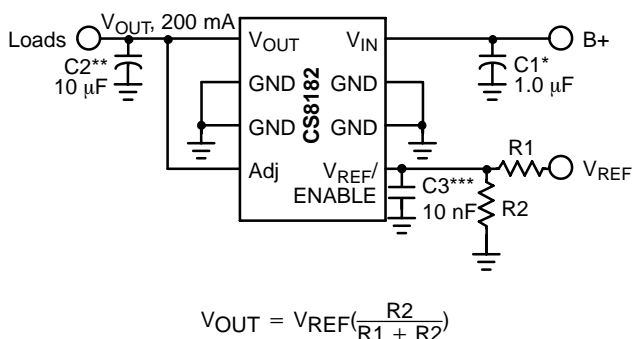


Figure 9. Tracking Regulator at Lower Voltages

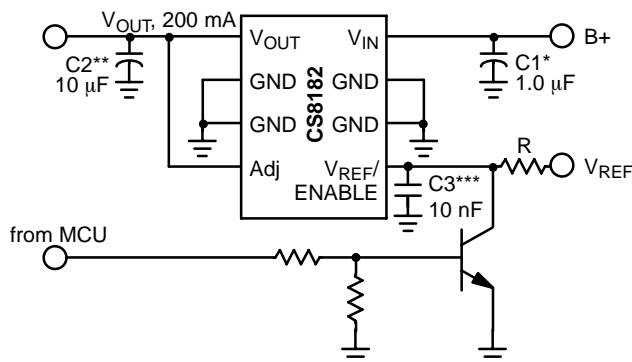


Figure 10. Tracking Regulator with ENABLE Circuit

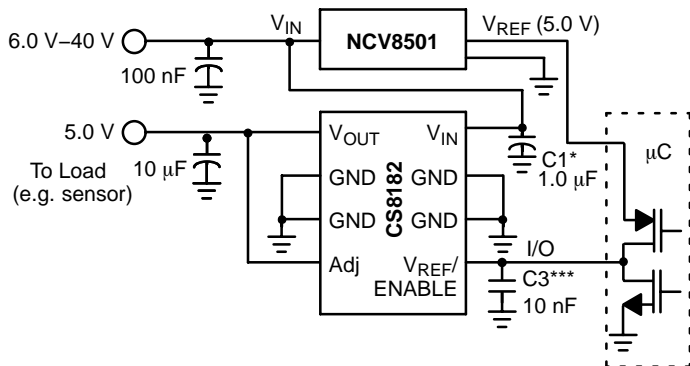


Figure 11. Alternative ENABLE Circuit

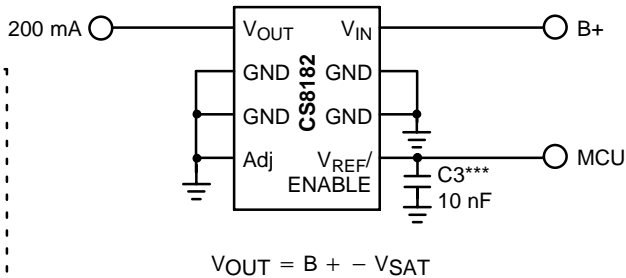


Figure 12. High-Side Driver

\* C1 is required if the regulator is far from the power source filter.  
 \*\* C2 is required for stability.  
 \*\*\* C3 is recommended for EMC susceptibility.

APPLICATION NOTES

**V<sub>OUT</sub> Short to Battery**

The CS8182 will survive a short to battery when hooked up the conventional way as shown in Figure 13. No damage to the part will occur. The part also endures a short to battery when powered by an isolated supply at a lower voltage as in

Figure 14. In this case the CS8182 supply input voltage is set at 7 V when a short to battery (14 V typical) occurs on V<sub>OUT</sub> which normally runs at 5 V. The current into the device (ammeter in Figure 14) will draw additional current as displayed in Figure 15.

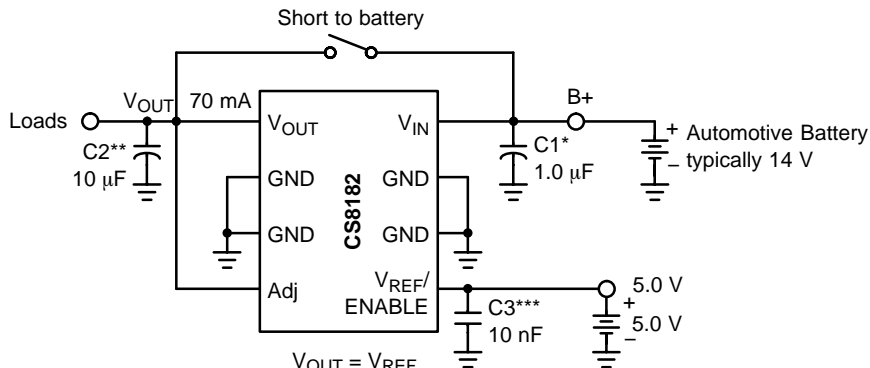
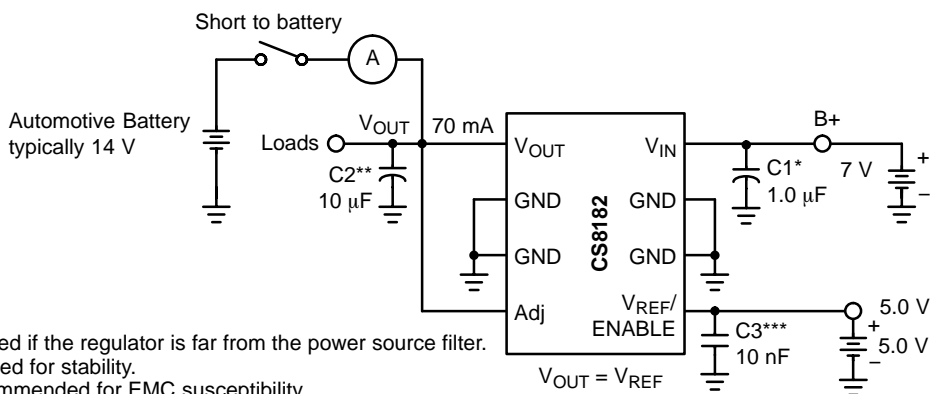


Figure 13.



\* C1 is required if the regulator is far from the power source filter.  
 \*\* C2 is required for stability.  
 \*\*\* C3 is recommended for EMC susceptibility.

Figure 14.

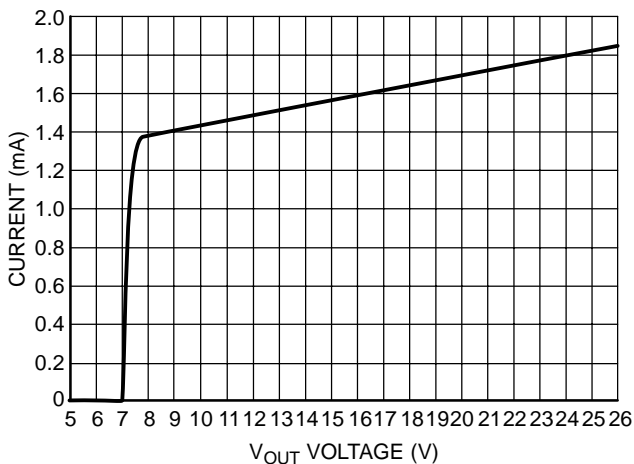


Figure 15. V<sub>OUT</sub> Short to Battery

**Switched Application**

The CS8182 has been designed for use in systems where the reference voltage on the V<sub>REF/ENABLE</sub> pin is continuously on. Typically, the current into the V<sub>REF/ENABLE</sub> pin will be less than 1.0 μA when the voltage on the V<sub>IN</sub> pin (usually the ignition line) has been switched out (V<sub>IN</sub> can be at high impedance or at ground.) Reference Figure 16.

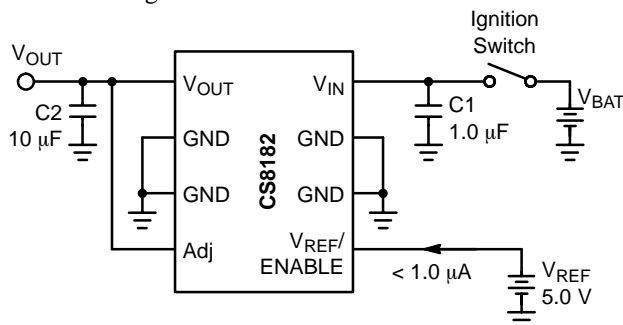


Figure 16.

**External Capacitors**

The output capacitor for the CS8182 is required for stability. Without it, the regulator output will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst-case is determined at the minimum ambient temperature and maximum load expected.

The output capacitor can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltage during brief conditions of negative input transients that might be characteristic of a particular system.

The capacitor must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to -40°C, a capacitor rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, “Compensation for Linear Regulators,” document number SR003AN/D, available through our website at <http://www.onsemi.com>.

**Calculating Power Dissipation in a Single Output Linear Regulator**

The maximum power dissipation for a single output regulator (Figure 17) is:

$$PD(max) = \{V_{IN(max)} - V_{OUT(min)}\} I_{OUT(max)} + V_{IN(max)} I_Q \tag{1}$$

where:

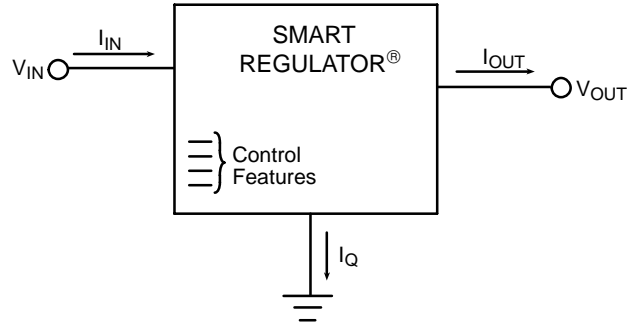
- $V_{IN(max)}$  is the maximum input voltage,
- $V_{OUT(min)}$  is the minimum output voltage,
- $I_{OUT(max)}$  is the maximum output current, for the application, and
- $I_Q$  is the quiescent current the regulator consumes at  $I_{OUT(max)}$ .

Once the value of PD(max) is known, the maximum permissible value of  $R_{\theta JA}$  can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}C - T_A}{P_D} \tag{2}$$

The value of  $R_{\theta JA}$  can then be compared with those in the package section of the data sheet. Those packages with  $R_{\theta JA}$ 's less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heat sink will be required.



**Figure 17. Single Output Regulator with Key Performance Parameters Labeled**

**Heatsinks**

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of  $R_{\theta JA}$ :

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \tag{3}$$

where:

- $R_{\theta JC}$  = the junction-to-case thermal resistance,
- $R_{\theta CS}$  = the case-to-heatsink thermal resistance, and
- $R_{\theta SA}$  = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$  appears in the package section of the data sheet. Like  $R_{\theta JA}$ , it is a function of package type.  $R_{\theta CS}$  and  $R_{\theta SA}$  are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heatsink manufacturers.

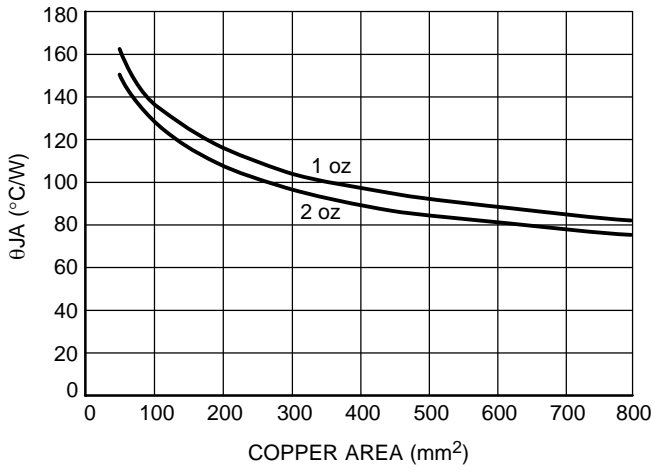


Figure 18. 8 Lead SOIC (Fused) Thermal Resistance

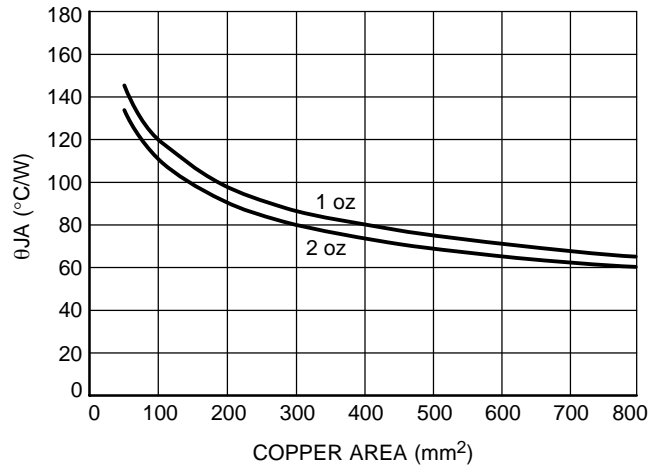


Figure 19. 5 Lead DPAK Thermal Resistance

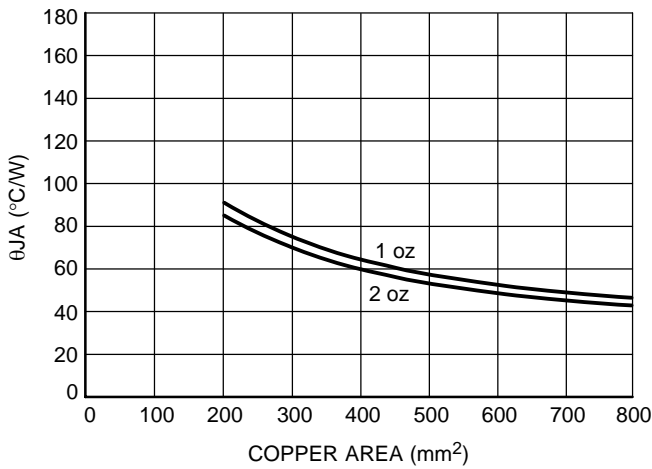


Figure 20. 5 Lead D<sup>2</sup>PAK Thermal Resistance

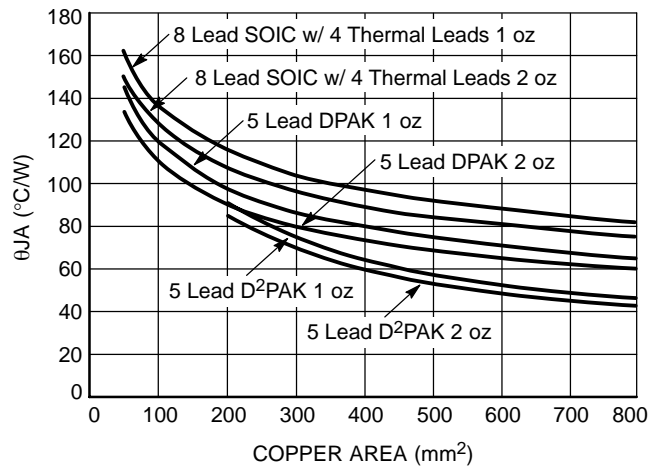


Figure 21. Thermal Resistance Summary



# CS8182

## ORDERING INFORMATION

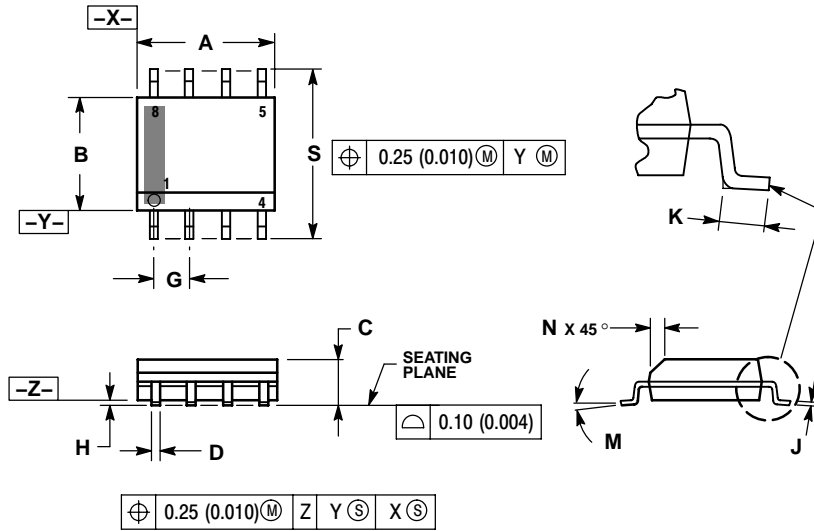
Device	Package	Shipping†
CS8182YDF8	SO-8	95 Units / Rail
CS8182YDF8G	SO-8 (Pb-Free)	95 Units / Rail
CS8182YDFR8	SO-8	2500 / Tape & Reel
CS8182YDFR8G	SO-8 (Pb-Free)	2500 / Tape & Reel
CS8182YDPS5	D <sup>2</sup> PAK 5-PIN	50 Units / Rail
CS8182YDPS5G	D <sup>2</sup> PAK 5-PIN (Pb-Free)	50 Units / Rail
CS8182YDPSR5	D <sup>2</sup> PAK 5-PIN	750 / Tape & Reel
CS8182YDPSR5G	D <sup>2</sup> PAK 5-PIN (Pb-Free)	750 / Tape & Reel
CS8182DTG	DPAK 5L (Pb-Free)	50 Units / Rail
CS8182DTRKG	DPAK 5L (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# CS8182

## PACKAGE DIMENSIONS

SOIC-8  
DF SUFFIX  
CASE 751-07  
ISSUE AG

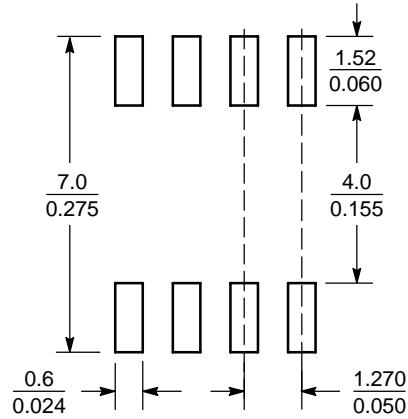


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



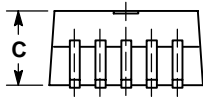
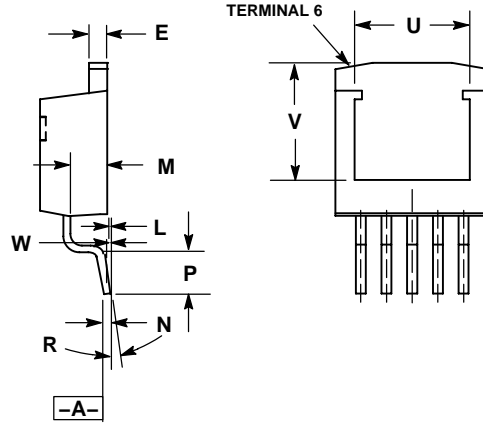
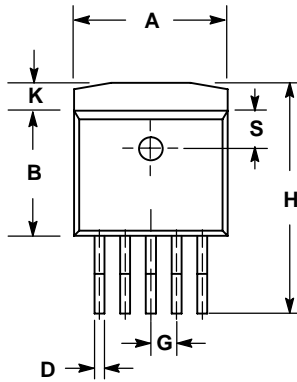
SCALE 6:1  $\left(\frac{\text{mm}}{\text{inches}}\right)$

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# CS8182

## PACKAGE DIMENSIONS

D<sup>2</sup>PAK-5  
 DP SUFFIX  
 CASE 936AC-01  
 ISSUE O



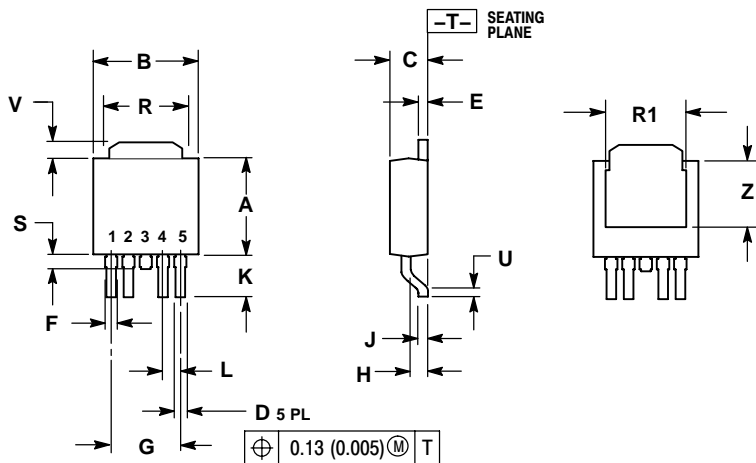
- NOTES:
1. DIMENSIONS AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH AND METAL BURR.
  4. PACKAGE OUTLINE INCLUSIVE OF PLATING THICKNESS.
  5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A AND LEAD SURFACE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.396	0.406	10.05	10.31
B	0.330	0.340	8.38	8.64
C	0.170	0.180	4.31	4.57
D	0.026	0.036	0.66	0.91
E	0.045	0.055	1.14	1.40
G	0.067 REF		1.70 REF	
H	0.580	0.620	14.73	15.75
K	0.055	0.066	1.40	1.68
L	0.000	0.010	0.00	0.25
M	0.098	0.108	2.49	2.74
N	0.017	0.023	0.43	0.58
P	0.090	0.110	2.29	2.79
R	0°	8°	0°	8°
S	0.095	0.105	2.41	2.67
U	0.30 REF		7.62 REF	
V	0.305 REF		7.75 REF	
W	0.010		0.25	

# CS8182

## PACKAGE DIMENSIONS

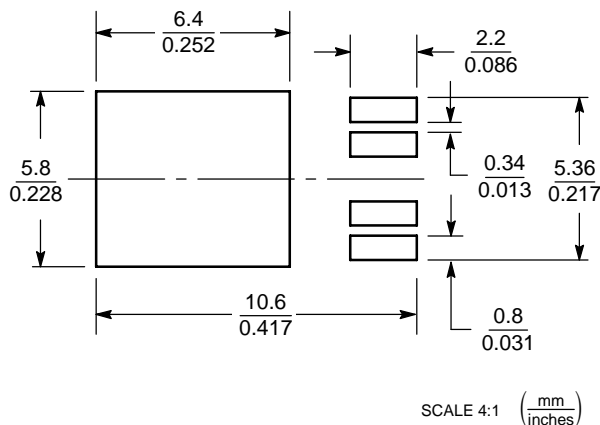
DPAK-5  
DT SUFFIX  
CASE 175AA-01  
ISSUE A



NOTES:  
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.22
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.020	0.028	0.51	0.71
E	0.018	0.023	0.46	0.58
F	0.024	0.032	0.61	0.81
G	0.180	BSC	4.56	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.102	0.114	2.60	2.89
L	0.045	BSC	1.14	BSC
R	0.170	0.190	4.32	4.83
R1	0.185	0.210	4.70	5.33
S	0.025	0.040	0.63	1.01
U	0.020	---	0.51	---
V	0.035	0.050	0.89	1.27
Z	0.155	0.170	3.93	4.32

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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